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Contents

Section

1.	Introduction	
1.1	Description of the Technology	1
1.2	Description of the Silicon-Film™ Products	1
1.3	Relationship of Silicon-Film™ Family Product Development to the PVMaT Program	3
2.	Description of Manufacturing Procedure (Task 1)	
2.1	Overall Process Flow Sheet	4
2.2	Silicon-Film™ Wafer Fabrication Process	5
2.3	Solar Cell Fabrication Process	5
2.4	Module Fabrication Process	6
3.	Description of Processes That Lead to Improvement (Task 2)	
3.1	Silicon-Film™ Wafer Fabrication Process	7
3.2	Solar Cell Fabrication Process	9
3.3	Module Fabrication Process	10
3.4	Long Range Potential Benefits of Improved Processes	10
4.	Problem Identification (Task 3)	
4.1	Silicon-Film™ Wafer Fabrication Process	11
4.2	Solar Cell Fabrication Process	11
4.3	Module Fabrication Process	12
5.	Approaches to Achieve Goals (Task 4)	
5.1	Silicon-Film™ Wafer Fabrication	13
5.2	Solar Cell Fabrication	14
5.3	Module Fabrication	14
5.4	Focus of Work in Phase 2	14
6.	Significant Work Performed During Contract	
6.1	Silicon-Film™ Wafer Fabrication	16
6.2	Solar Cell Fabrication	16
	References	17

Section 1

Introduction

1.1 Description of the Technology

The Silicon-Film™ process is being developed with the objective of achieving a high-performance, low-cost solar cell for terrestrial power applications. The approach is guided by device modeling. A high performance device structure has been designed which can be fabricated from imperfect materials. The technical approach involves development of a technique for preparing crystalline silicon on a low cost substrate. The commercial feasibility of this approach has been demonstrated by the achievement of a 100 cm², 10.9% commercial-size solar cell.

The Si-Film device incorporates a thin (30 to 100 micron) silicon layer on a low cost substrate. To optimize performance in a thin device structure, light trapping and back surface passivation must be incorporated. When fully optimized, the Si-Film device structure will outperform the conventional 400-micron thick silicon solar cell.

The achievement of high levels of light-generated current in conventional devices requires long diffusion lengths (>300 microns) to retrieve carriers generated deep in the bulk. In a thin device design this requirement is greatly reduced. A diffusion length on the order of twice the device thickness is satisfactory for charge carrier retrieval [1]. For devices with Si-Film layers 30 microns thick, a 60 micron diffusion length is sufficient. The reduced diffusion length requirement allows higher levels of impurities to be present in the silicon. This relaxation of silicon quality allows greater flexibility in processing. Since thinner devices allow gettering to be much more effective, impurity effects can be further minimized.

1.2 Description of the Silicon-Film™ Products

The development of the Si-Film process has generated a family of three products. They are pictured in Figure 1. Product I, which is presently in production, utilizes a 100 micron thick active layer of silicon on a low cost supporting substrate. There is no barrier layer between the active layer and the substrate, and no light trapping features are designed in the structure. A recent review of the production development of Product I [2] reported an efficiency range of 6.8% to 10.9% in an initial series of 100-cm² solar cells.

Light trapping and back surface passivation are incorporated into the Product II design

shown in Figure 1. Product II differs from Product I by the presence of a metallurgical barrier layer, and by the reduction in thickness of the active silicon layer to 30 microns. The metallurgical barrier (MB) layer plays an important role in the thin device design. The reduction of recombination at the back surface is critical to the overall device efficiency and is dependent on the properties of the Si-Film/MB interface. An effective light trapping design requires that the interface be reflective to confined light. Additionally, the metallurgical barrier must have the mechanical strength to withstand the silicon deposition process, while not introducing impurities that may have a deleterious effect on device performance. The fully engineered Product II solar cell is expected to achieve a conversion efficiency in excess of 19% [1].

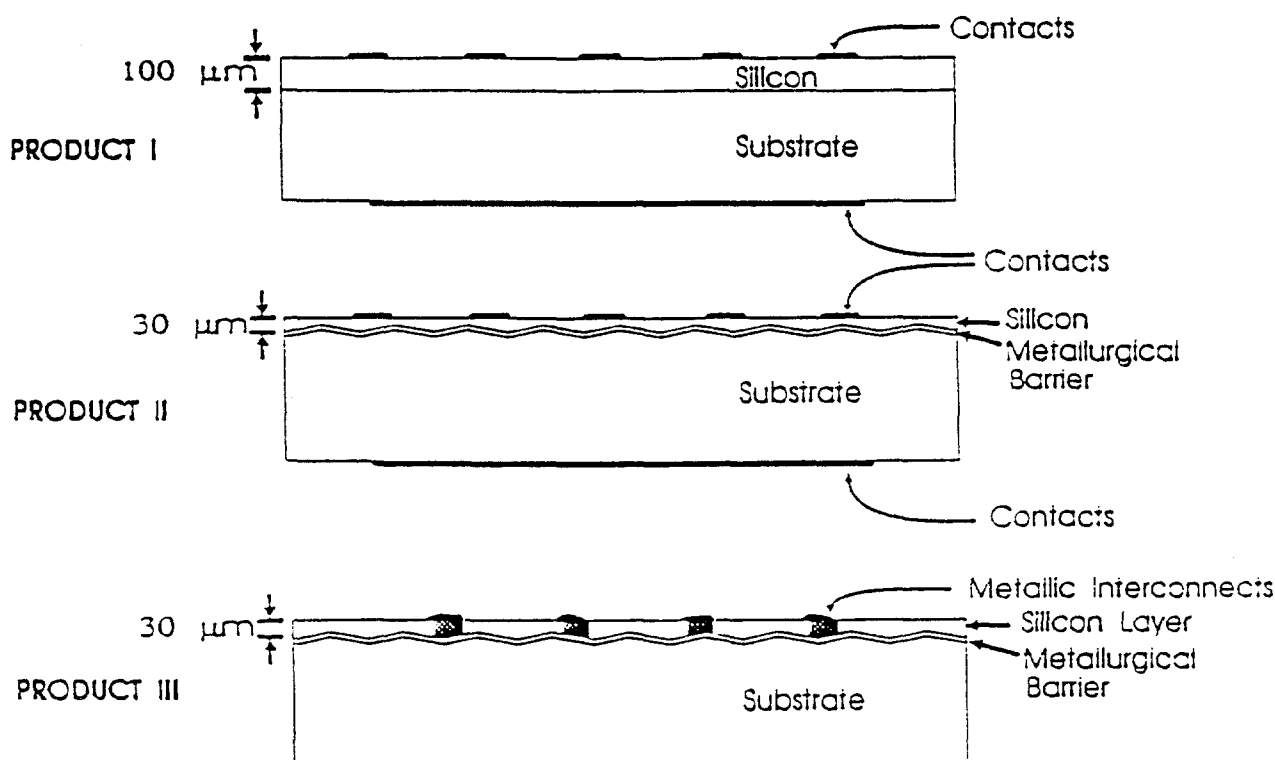


Figure 1. Silicon-Film™ Product Families.

Product III utilizes the Si-Film process developed for Product II, therefore enjoying the performance and cost benefits of the thin silicon light trapping design. The active silicon layer is configured into a monolithically integrated, high-voltage structure. This structure allows all electrical contacting to be made on the back of the device, therefore simplifying module assembly. The high-voltage, low-current configurations possible with such a device minimize contact resistance problems and avoid front surface shadowing by current carrying metallic grids. The Product III design allows the use of the large ceramic substrates (10cm x 60cm) generated by the Si-Film process. In terms of product development maturity, Product II trails Product I by three years, and Product III is three years behind Product II.

1.3 Relationship of Silicon-Film™ Family Product Development to the PVMaT Program

AstroPower has generated a clear plan for the development of the Silicon-Film™ technology. This plan allows entry into the market with a reliable, cost effective product, Product I, followed by a sequence of improved products utilizing the experience gained with each introduction. The introduction of Product I is not controlled by the development of new science or technology, but by the development of manufacturing technology using known engineering principles. The rate of introduction of these products will be controlled by the availability of suitable engineering data and its application to the problems at hand.

It is expected that PVMaT will have a significant impact on the rate of development of Product I for utility scale applications by providing a focus for the engineering issues of production advancement. The following sections of this report describe the important engineering issues related to scaling up a proven technology concept.

Section 2

Description of Manufacturing Procedure (Task 1)

2.1 Overall Process Flow Sheet

A general overview of the manufacturing process for Silicon-Film™ Modules is shown in Table 2.1.

The manufacturing process description contained in this report does not contain proprietary information.

There are three primary stages in the manufacture of a module using Silicon-Film™ wafers: wafer formation, solar cell fabrication and module fabrication. The process steps after wafer fabrication are almost identical to those found in the conventional single crystal or polycrystalline silicon technologies. A more detailed description of each major process follows in the next sections.

Table 1

Product I Si-Film Wafer, Solar Cell and Module Process		
Wafer Formation	Solar Cell Formation	Module Formation
1) Compound materials	5) Surface Preparation	12) Tab solar cells
2) Form substrate	6) Diffuse, strip, plasma etch	13) String cells and circuits
3) Grow Silicon-Film	7) Screen print, fire back contacts	14) Lay-up laminate
4) Size Wafer	8) Screen print, fire front contacts	15) Vacuum laminate
	9) AR coat	16) Apply edge seal
	10) Burnish contacts	17) Apply junction box
	11) Test	18) Test

2.2 Silicon-Film™ Wafer Fabrication Process

The first of the proprietary steps in the fabrication of Si-Film wafers is the substrate formation step. This step involves the fabrication of a low cost substrate with suitable properties to support subsequent processing, but to not deleteriously affect device operation.

The Si-Film Product I, presently in Pilot Scale Production, does not require a metallurgical barrier.

The final proprietary Si-Film wafer fabrication steps involve the sequential application and formation of the photovoltaic silicon layer. A silicon solution is formed which covers the substrate. The photovoltaic properties of the grown layer are enhanced using a process employing a prescribed thermal profile. In the present Product I prototype the active silicon layer is approximately 100 microns thick. The overall thickness of the Si-Film wafer is 500 microns for both the Product I and II structures.

These wafers are distinguishable from conventional crystalline wafers in that only the side with the thin photovoltaically active silicon can be usefully employed for solar cell fabrication. Other than this the solar cell fabrication process steps are identical to those used for conventional wafers.

The equipment necessary to carry out the first step of the Si-Film wafer fabrication process is commercially available, although modifications to accommodate the specific process are required. The equipment to effect the active layer application and Silicon-Film™ growth steps is not commercially available. The processes employed in these two steps were developed to accomplish specific features of the Si-Film process, and accordingly the equipment required development as well. An analysis of the laboratory-scale process, that was employed to produce the commercial-scale Product I prototype solar cells, has been carried out to formulate a process specification. This process specification was used to design a commercial-scale process for the application and formation of the active layer of the Product I Si-Film wafer.

During the last year an initial pilot version of a commercial-scale process for the fabrication of Product I Si-Film wafers has been designed, fabricated and is presently being operated. More recently the first production equipment was brought on-line. A subsequent sizing step converts the silicon sheet material into properly sized wafers suitable for solar cell fabrication.

2.3 Solar Cell Fabrication Process

Solar cells are made from the Silicon-Wafers using a conventional crystalline silicon process sequence. The p-type, boron doped wafers are cleaned in a series of caustic and acid etch steps to prepare a clean surface for diffusion. Phosphorus containing material is used as an n-type dopant to produce a junction with a nominal thickness of 0.25 μ . The junction is removed from the edges of the wafer in a plasma etch step. The phospho-silicate glass is removed from the

wafer surface with an HF acid etch. Front and back contacts are applied by screen printing a silver containing ink employing an optimized contact pattern. The ink is fired into the surface to make ohmic contact using an infra-red firing furnace. A metal oxide antireflection coating is applied. The index of refraction and thickness of the coating is matched to optimize optical throughput of light in the solar spectrum weighted by the response of the solar cells. The contacts are burnished to remove the metal oxide coating in order to allow easy soldering of the interconnect ribbons to the contact trace. The finished solar cells are 100% tested on automatic testers and sorted into current matched bins.

2.4 Module Fabrication Process

Module fabrication is carried out using a conventional flat-plate module design for crystalline silicon solar cells. A series connected string of 36 solar cells is laminated onto a 17.5" x 38" piece of tempered, low iron glass. The cells are interconnected with solder coated copper ribbon which is soldered to the silver front and back contacts. Two interconnect ribbons are provided along the length of the cell to provide a dual/redundant interconnect design. Ethylene vinyl acetate, EVA, is used as the plastic lamination material. The back is protected using a 4 mil thick layer of tedlar bonded to the laminate during encapsulation. A junction box is bonded to the back of the laminate. An aluminum frame captures the laminated sheet to give structural integrity to the sheet, to protect the edge of the laminate and to provide locations for attachment to array structures. This design is based on technology widely used to meet the JPL Block V specification.

Section 3

Description of Processes That Lead to Improvement (Task 2)

3.1 Silicon-Film™ Wafer Fabrication Process

There are four generic issues that relate to improvement in the cost effectiveness of crystalline silicon technology. These are: 1. silicon material use efficiency, 2. use of silicon of lower purity, 3. achievement of high production rates, and 4. improvements in solar cell efficiency. Silicon-Film™ technology uniquely offers the opportunity to meet these requirements.

Wafers fabricated using the conventional single crystal or cast polysilicon technologies will not be cost effective for future high volume, low cost applications. Material use efficiency for these technologies is 40-50% because of the requirement to saw ingots and blocks. The wafers fabricated using older processes are in the range of 350-400 μ thick. Newer sawing process produce wafers in the range of 180-220 μ . Efficient current collection requires that the diffusion length be greater than the wafer thickness. Thus, all thick silicon wafers require high quality silicon. Silicon wafer production rates are slow and limited because of the large thermal mass of the material and reactor, and because of the requirement of sawing ingots or blocks into wafers. In addition, capital costs are high for pullers, block casters and saws. The wafer forming process developed by AstroPower addresses these issues by the use of Silicon-Film™ technology. The Silicon-Film™ wafer forming process is an integrated sequence described in the previous section.

As shown in Tables 3.1 and 3.2, solar cells fabricated from Silicon-Film™ wafers show a path to achieve high efficiency while lowering material usage, eliminating ingot sawing and offering the potential for achieving high production rates. The fabrication of >10% solar cells on 10cm by 10cm substrates using this basic process shows the potential for achieving the requirements for manufacturability at high volumes and low cost.

Table 3.1

Improvements in Wafer Fabrication Technology with Silicon-Film™

<u>Issue/Problem</u>	<u>Improvement</u>	<u>Goal</u>
Conventional material using thick active layers achieves material usage of ~40%	Increase silicon material use efficiency	90+%
Conventional requires high purity silicon	Employ device design that allows utilization of lower quality silicon	$L_n < 100 \mu$
Conventional growth rates are slow and require expensive equipment	Increase wafer fabrication rate	$>240 \text{ cm}^2/\text{min}$

Table 3.2

Specific Process Features Showing Improvements with Silicon-Film™

<u>Issue</u>	<u>Process Features</u>
Material usage	Grow thin active layer, $<100 \mu$ Use inexpensive substrate Avoid sawing
Lower quality material	Thin active layer requires only that $L_n > \text{thickness}(t)$
Growth rate	Stable process for equilibrium growth
Efficiency	Grow large grains in active layer, $l_G > 2 L_n$ Grow thin active layer, $t < L_n$

The specific process in wafer fabrication that will lead to improvements is the Silicon-Film™ growth process. Three areas have been identified which will improve the cost effectiveness of the technology: increase in wafer machine productivity, reduction of material

usage and improvement of material quality.

Wafer machine productivity. Machine productivity will be increased by steadily increasing the linear growth rate and machine growth width.

Material usage. The growth process will be tuned to accommodate decreasing the active layer thickness.

Improvement of material quality. Improvements in the usage of silicon material by reduction in active layer thickness and improvements in deposited grain quality will continue and improve the ability to use lower quality silicon.

3.2 Solar Cell Fabrication Process

The key solar cell fabrication issue for reducing cost and maintaining performance is the achievement of high efficiency while simultaneously using lower quality material. An essential feature in the development of Silicon-Film™ technology is that most of the conventional processes for crystalline silicon solar cell fabrication can be carried over with little change. The baseline process sequence has been discussed in Section 2. Pilot production experience supports the contention that few modifications will be required in the process sequence, and that the sequence may become simpler.

Three areas have been identified which will improve the cost effectiveness of the technology: solar cell efficiency improvement, reduction in materials usage and automation. Specific process steps that will be examined for each improvement area are described below.

Solar cell efficiency improvement. The diffusion process will be tuned to obtain an optimal profile for blue response, front contact equivalent resistance, front contact obscuration and surface passivation. The AR coating process will be tuned to collect the maximum amount of light. Several schemes for passivation and gettering of impurities will be considered. The crucial issue for the latter improvements will be the potential for high volume application.

Material usage. We will investigate reduction of contact materials in high volume printer applications. Surface preparation times will be minimized and material costs lowered because saw damage etching will not be required.

Automation. Advanced concepts in wet chemical processing will be explored. The goal will be to reduce the materials usage, waste generated and increase the production rate. These processes are presently batch oriented, while modern manufacturing is evolving towards continuous processing. High speed screen printing of contacts will be integrated with the Silicon-Film™ solar cell process.

It is expected that part of the Phase 2 work will focus on matching the solar cell

fabrication process to the characteristics of the Silicon-Film™ wafers. The goal is to produce solar cells with superior output at lower cost.

3.3 Module Fabrication

Module manufacture employs the same techniques used in crystalline silicon processes as described in Section 2. This is because Silicon-Film™ solar cells are plug-to-plug compatible with conventional crystalline silicon wafers. Significant effort will be expended in the proposed program to reduce the cost of module manufacture.

Several areas have been identified for improvement: automation of the circuit formation process, reduction in materials costs, increasing process productivity.

Automation of circuit formation. The multi-step process of tabbing, string formation and lay up will be replaced with an integrated circuit formation process.

Reduction in materials costs. Panels designed for utility applications require a different set of framing and termination hardware than required for commercial or consumer applications. In the PVMaT Phase 2 program we will design and demonstrate modules and panels that minimize the material and installation costs for arrays.

Process productivity. Use of larger cells will reduce the labor and material costs related to handling of piece parts. We will develop and demonstrate manufacturing processes which will accommodate larger solar cells.

3.4 Long Range Potential Benefits of Improved Processes

The barrier to the penetration of utility markets by photovoltaic technology is the high cost of manufacture in terms of dollars per watt. The work proposed for Phase 2 of the program will improve the Silicon-Film™ wafer forming and solar cell fabrication process steps by increasing equipment productivity, reducing material usage, minimizing capital investment, increasing solar cell efficiency and increasing product efficiency.

The ultimate benefit of long-term research on improvement of the Silicon-Film™ wafer manufacturing process and the reduction of manufacturing costs will be the penetration into the utility power markets by these advanced products.

Section 4

Problem Identification (Task 3)

4.1 Silicon-Film™ Wafer Fabrication Process

As described in the previous section the objectives for developing improved wafer fabrication manufacturing technology are reduction in material usage, use of lower purity silicon and achievement of high throughput rates while maintaining high efficiency in the finished solar cell. AstroPower has shown that these objectives are feasible employing commercial scale processing equipment. However there are barriers to achieving the goals required to penetrate the utility market. The demonstrated rates which yield high efficiencies are too slow to be acceptable for low cost, high volume production. The specific problem is to maintain uniform growth of the thin active layer with large grain size. Another problem requiring solution is determining the optimal size for replicating the basic Silicon-Film™ wafer fabrication building-block. This is important in order to minimize capital costs.

Several problems related to increasing the growth rate while maintaining good crystal morphology and thickness can be identified. The rate is determined by two primary factors: control of instabilities in the growth zone and control of the direction and rate of heat removal from the growth zone. These factors are under control in the present, commercial production machine. The material grown makes acceptable solar cells and has under certain conditions made greater than 10% solar cells on 10cm by 10 cm substrates [2]. The present system is operated under open-loop control conditions. The achievement of higher growth rates and high wafer yields will require the development of a closed-loop control system which will control the primary operating parameters.

The problem of minimizing capital equipment costs depends on two factors. The first factor is linear processing rate. The second factor is the design of the optimal machine configuration to take advantage of opportunities for parallel operation. At present the range of values for operating parameters is not well enough known to design standard production machines. It is important to gather detailed operating data on the present commercial production machine.

4.2 Solar Cell Fabrication Process

As discussed in Sections 2 and 3 the development of Silicon-Film™ wafers retains the utility of the crystalline silicon solar cell production technology with its proven capability to produce high efficiency solar cells at known costs. The effort required in the campaign to reduce cost using Silicon-Film™ technology will focus on the following problems: electrical performance, material usage and labor content.

The first target will be to adjust the solar cell processes to the characteristics of Silicon-

Film™ material. The specific processes to be optimized are diffusion, contact printing and AR coating. In addition there are opportunities to employ surface passivation and gettering processes to improve performance. The technical problem will be to obtain manufacturable processes.

The second target will be to minimize material usage in the process steps. Process steps identified that require work are contact print/fire and wet etch steps. These steps use the bulk of the materials consumed during solar cell processing.

The third target will be to reduce labor content by advanced automation. AstroPower is currently developing process stations with high throughput rates with minimal operator attention. As part of the PVMat program AstroPower will accommodate changes in these process stations to the requirements of Silicon-Film™ wafers.

4.3 Module Fabrication Process

The initial modules made using Silicon-Film™ technology will be based on standard crystalline silicon module fabrication technology. The long range problem with this technology is its high material cost content and labor content. The module consists of a glass superstrate laminated with a thermosetting plastic and the solar cell circuit. Modules for many consumer and commercial applications require frames for mounting and edge protection and require complicated junction boxes to serve many different interconnection needs. The specific problem to be solved is the reduction of high materials cost component in module manufacture. AstroPower proposes to develop modules suitable for panels to be incorporated into arrays.

The second problem to be solved is the reduction of labor cost in module manufacture. The present process requires hand tabbing, circuit stringing and lamination lay-up. High volume manufacture requires the integration and automation of these tasks.

Section 5

Approaches to Achieve Goals (Task 4)

5.1 Silicon-Film™ Wafer Fabrication

There are four specific stages that will be accomplished to solve the problems discussed in Section 4:

1. Establish Silicon-Film™ Product I performance and yield employing the existing commercial production machine.
2. Develop a closed-loop control scheme for the silicon application and active layer formation process steps.
3. Determine throughput levels that can be achieved with the process consistent with the maintenance of product performance and yield.
4. Determine the optimal capacity of the basic building-block system for producing Silicon-Film™ Product I wafers. Plan and implement the strategy to replicate the block to achieve production rate goals.

The performance of Si-Film Product I wafers will depend upon obtaining silicon layers with the proper morphology, grain-size, thickness and doping levels. The prototype silicon application and formation apparatus has several process variables that are employed to control the product quality. These process variables are being used along with solar cell processing methods to optimize solar cell performance. The system yield is dependent on establishing the capability to handle product in a continuous manner and controlling the process to produce product with required performance characteristics. These two factors determine mechanical and quality yields respectively.

The first stage will be to establish a performance benchmark for the Silicon-Film™ wafer process. The development of a closed-loop control system for selected process variables will be necessary to establish quality yields on the Silicon-Film™ prototype apparatus. The throughput level of a single generic Si-Film Product I processing system is determined by the linear process rate and the number of units (wafers) which can be run in parallel through the system. Since the product cost generally varies inversely with process throughput, a determination of the processing boundary conditions controlling product performance is necessary.

Once the parameter space controlling throughput of a single system producing high yield, high performance Si-Film Product I is reached, it becomes necessary to formulate a strategy to replicate the optimal process block to achieve high volume production goals.

5.2 Solar Cell Fabrication

Solar cell fabrication costs will be reduced by increasing the energy conversion efficiency, reducing some of the contact materials and other chemical costs and reducing the labor costs with advanced mechanization. AstroPower will complete this part of the manufacturing development as part of its contribution to cost sharing.

5.3 Module Fabrication

Module material and fabrication costs can be substantially reduced by using an integrated module design based on injection molding. The goal of the design is to include as many of the structural and functional features of the module as possible in a single molding/lamination process. The features which can be easily integrated include the support frame, the edge seal and the junction box. The automotive industry commonly uses this approach for fabricating windshields that incorporate defrosting features. AstroPower intends to team with material vendors to develop this module technology in the next three years.

Labor costs can be substantially reduced in two ways. The first is to employ the integrated module approach described above which reduces the number of operations. The second approach will be to build automatic circuit fabrication machines.

Finally, module costs can be reduced by increasing the size of the solar cell. This gains economy of scale per solar cell used in a module for labor and material usage costs.

5.4 Focus of Work in Phase 2

AstroPower proposes a three year plan to achieve the following objectives:

- 1) Improve the productivity of the Silicon-Film™ machine which will lead to reduced wafer costs
- 2) Reduce the materials consumption and increase the materials yield in the Silicon-Film™ wafer leading to further reductions in cost.
- 3) Improve the performance of the solar cells
- 4) Decrease the materials consumption in solar cell fabrication process and increase the mechanization leading to reduced cost
- 5) Decrease module cost by integrating and mechanizing the fabrication of modules from solar cells
- 6) Increase the size of the solar cell and module to reduce cost.

To accomplish these objectives AstroPower proposes during the first year to establish a benchmark process capability, identify wafer process boundary conditions and fabricate modules. During the second and third year the process capability identified during the first year will be established with production machines. Solar cell process improvements will be carried out during the first and second years of the program. Solar cell and module process automation will proceed during the second and third year of the program.

The level of effort required to carry out these tasks during the three year will be 8-10 million dollars.

Section 6

Significant Work Performed During Contract

6.1 Silicon-Film™ Wafer Fabrication

- * Completed the design and fabricated a production machine.
- * Detailed analysis performed of manufacturing cost dependent on: material cost, material usage, production rates and resultant solar cell performance.

6.2 Solar Cell Fabrication

- * Fabricated solar cells which are being used for module qualification for PVUSA program.

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16. Abstract (Limit: 200 words) This report describes the development of a process for preparing thin crystalline silicon on a low-cost substrate. Three cells derived from this process are described; two incorporate light trapping and back surface passivation. Wafer, solar cell, and module fabrication processes and improvements of those processes by using the wafer forming process developed by AstroPower also are described. Solar cells fabricated from AstroPower's Silicon-Film wafers use less material, eliminate ingot sawing, and have the potential to achieve high production rates. Problems in fabrication processes are identified and their solutions are explained. AstroPower proposes a 3-year plan (Phase 2) to develop a high-performance, low-cost solar cell used for terrestrial power applications.			
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